WHAT IS CLAIMED IS:

1. A semiconductor wafer polishing pad comprising a polishing layer and a cushion layer, wherein the polishing layer is formed from foamed polyurethane, has a flexural modulus of 250 to 350 MPa, the cushion layer is formed from closed-cell foam and has a thickness of 0.5 to 1.0 mm and a strain constant of 0.01 to 0.08 $\mu m/(gf/cm^2)$.

2. The polishing pad according to Claim 1, wherein the foamed polyurethane has an average cell diameter of 1 to 70 μm.

3. The polishing pad according to Claim 1 or Claim 2, wherein the foamed polyurethane has a specific gravity of 0.5 to 1.0 g/cm^3.

4. The polishing pad according to anyone of Claims 1 to 3, wherein the foamed polyurethane has a hardness of 45 to 65.

5. The polishing pad according to anyone of Claims 1 to 4, wherein the foamed polyurethane has a compressibility of 0.5 to 5.0%.

6. The polishing pad according to anyone of

Claims 1 to 5, wherein the cushion layer is formed from at least one material selected from the group consisting of polyurethane resin and polyethylene resin.

7. A method of producing a semiconductor device comprising at least a step of polishing the surface of the semiconductor wafer by using the polishing pad according to anyone of Claims 1 to 6.